Fig. 1

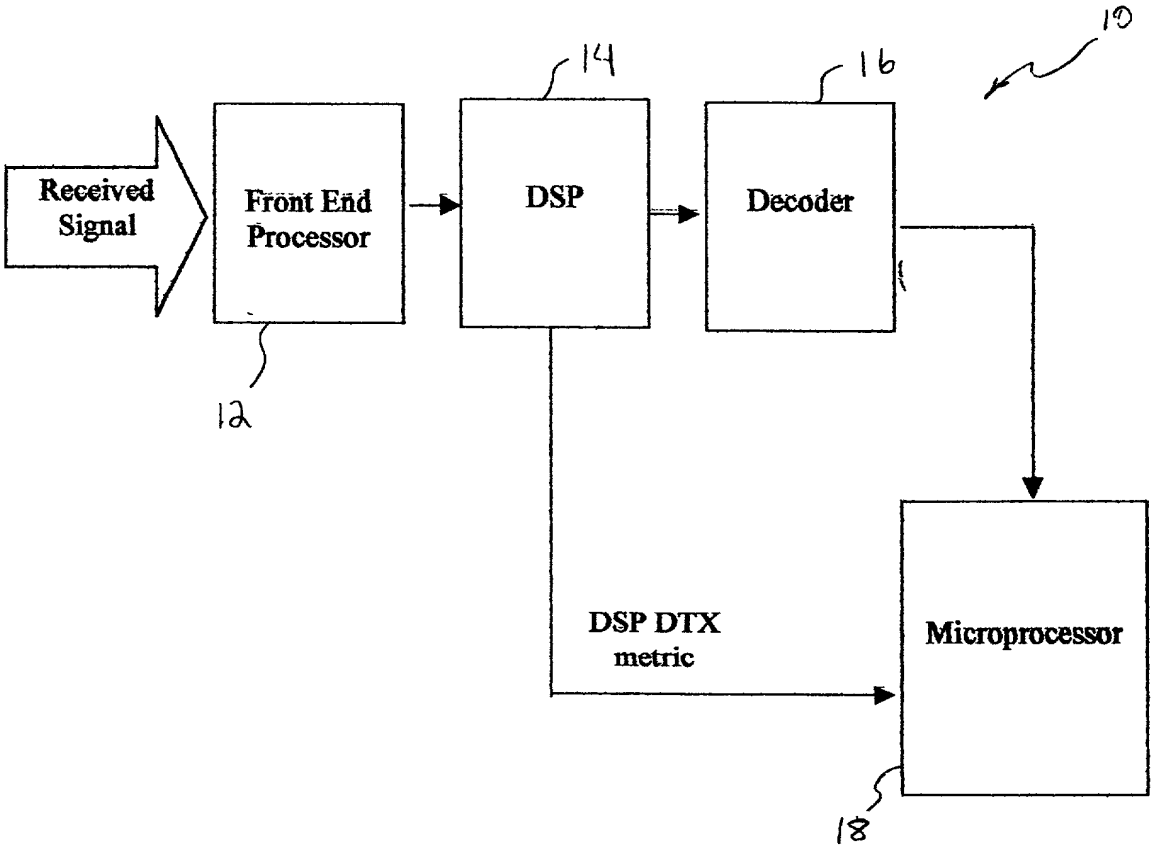

10
14
16
Received Signal
Front End Processor
DSP
Decoder
12
DSP DTX metric
Microprocessor
18

Fig. 2

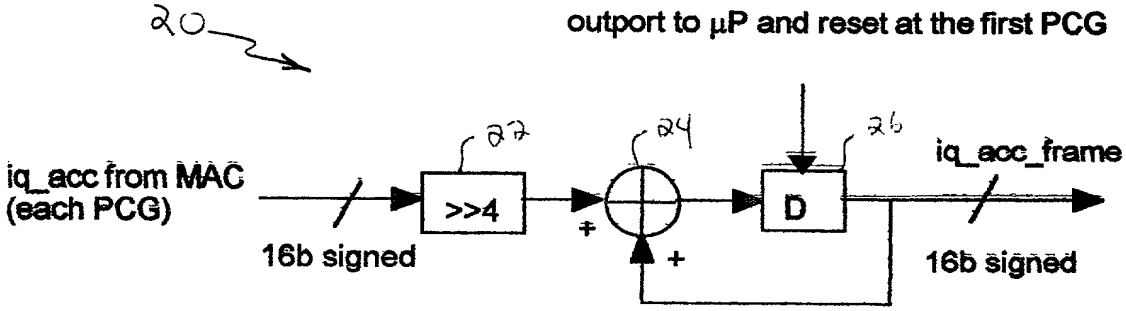

20
outport to µP and reset at the first PCG
22
24
26
iq_acc from MAC (each PCG)
>>4
D
iq_acc_frame
16b signed
+
+
16b signed

Fig. 3

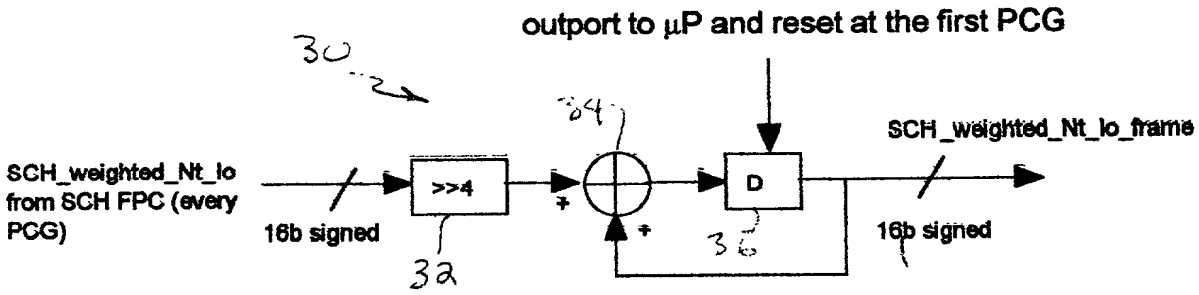

outport to μP and reset at the first PCG
30
34
SCH_weighted_Nt_Io from SCH FPC (every PCG)
16b signed
>>4
32
+
+
D
36
SCH_weighted_Nt_Io_frame
16b signed

Fig. 4

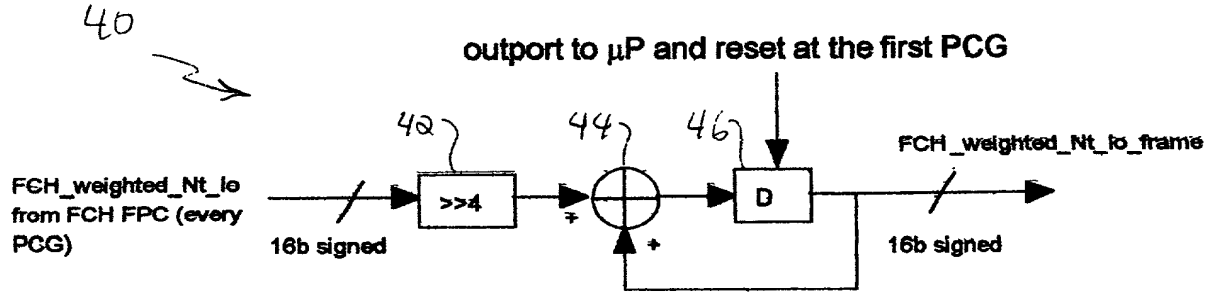

40
outport to μP and reset at the first PCG
42
44
46
FCH_weighted_Nt_Io from FCH FPC (every PCG)
16b signed
>>4
+
+
D
FCH_weighted_Nt_Io_frame
16b signed

Fig. 5

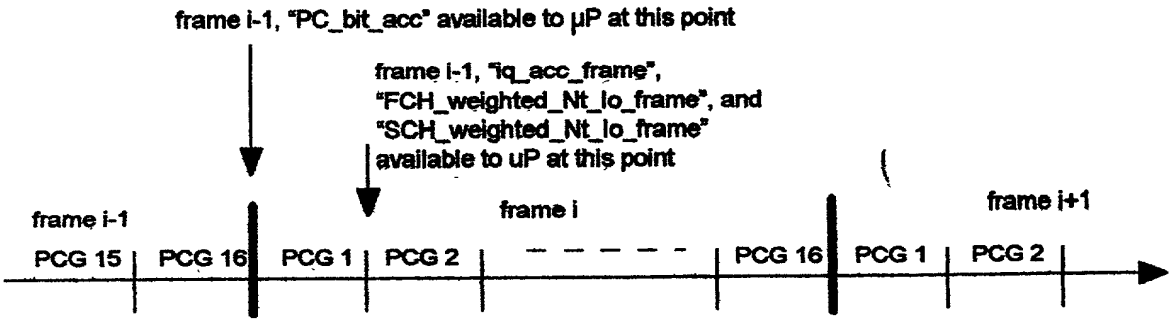

frame i-1, "PC_bit_acc" available to μP at this point
frame i-1, "iq_acc_frame", "FCH_weighted_Nt_Io_frame", and "SCH_weighted_Nt_Io_frame" available to uP at this point
frame i-1
frame i
frame i+1
PCG 15
PCG 16
PCG 1
PCG 2
PCG 16
PCG 1
PCG 2

Fig. 6

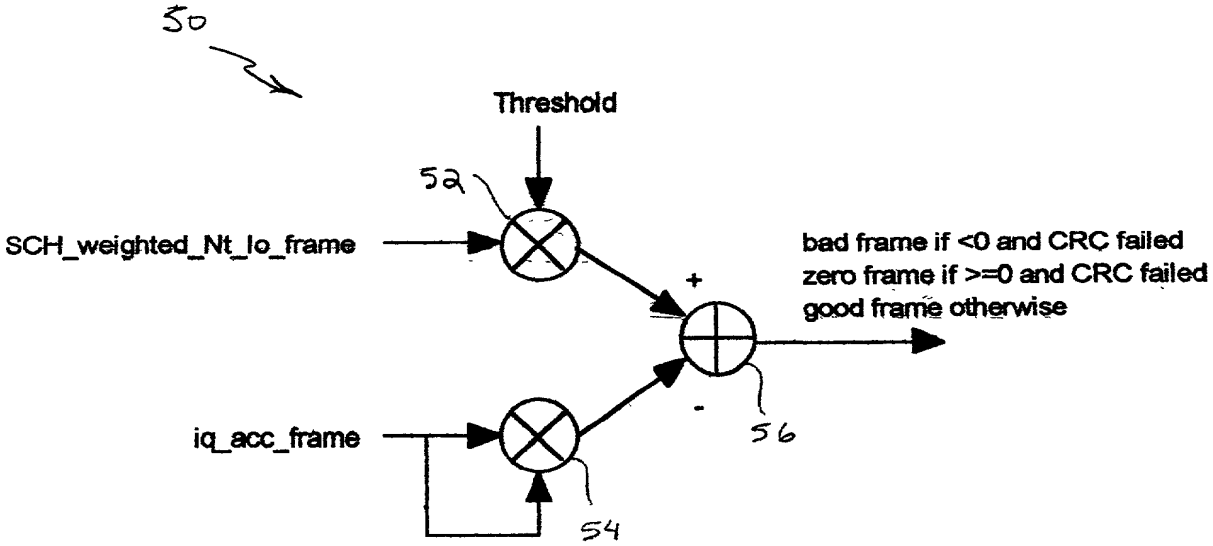
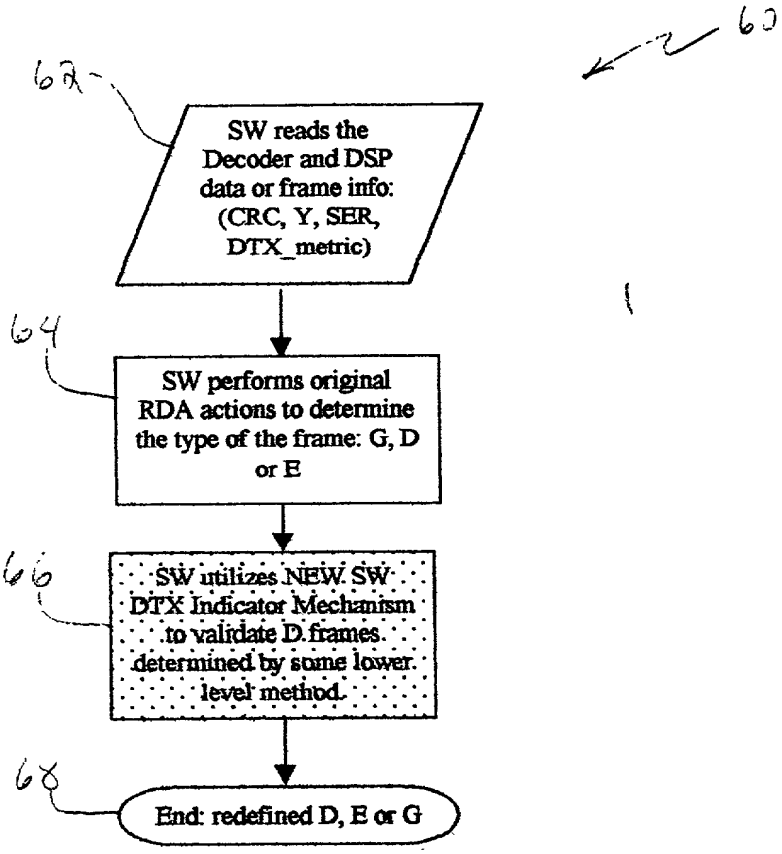

50
Threshold
52
SCH_weighted_Nt_Io_frame
bad frame if <0 and CRC failed
zero frame if >=0 and CRC failed
good frame otherwise
+
-
iq_acc_frame
56
54

Fig. 7


60
62
SW reads the Decoder and DSP data or frame info: (CRC, Y, SER, DTX_metric)
64
SW performs original RDA actions to determine the type of the frame: G, D or E
66
SW utilizes NEW SW DTX Indicator Mechanism to validate D frames determined by some lower level method.
68
End: redefined D, E or G